METHODS FOR REDUCING BITLINE VOLTAGE OFFSETS IN MEMORY DEVICES

ABSTRACT OF THE DISCLOSURE

A method of designing a memory device that has substantially reduced bitline voltage offsets is provided. The method includes providing a memory core having a depth that defines a plurality of words, and a word width that is defined by multiple pairs of a global bitline and a global complementary bitline. The method also includes designing a core cell having a bitline and a complementary bitline, and designing a flipped core cell that has a flipped bitline and a flipped complementary bitline. Further, the method includes arranging a core cell followed by a flipped core cell along each of the multiple pairs of the global bitline and the global complementary bitline. Preferably, the bitline of the core cell is coupled with the flipped complementary bitline of the flipped core cell, and the complementary bitline of the core cell is coupled to the flipped bitline of the flipped core cell.